Amendments to the Specification:

Please replace the paragraph at page 9, lines 19-23 with the following amended paragraph:

A1

Accordingly, the memory controller 40 recognizes the read data DQ arrival time via the RFLAG signal output by the C/A buffer 46A. The RFLAG signal preferably has the same propagation delay time as the read data DQ signals as the line on which the RFLAG signal is transported is preferably configured to be routed with, and therefore have the same propagation delay as the ~~return~~ read clock RCLK and data bus DQ signals.

Please replace the paragraph at page 10, lines 7-15 with the following amended paragraph:

A2

In the case of a data read operation, the data buffer 48 receives read data DQ in synchronization with a module read clock signal RCLK_MDL that is generated based on the module write clock signal WCLK_MDL received by the memory devices 44. [[.]] Next, with reference to FIG. 1 and FIG. 2, the data buffer 48 outputs the buffered read data DQ to the memory controller 40 in synchronization with the read clock signal RCLK_OUT generated by the first module 42A based on the input write clock signal WCLK_IN. Alternatively, in the case of a second module 42B, the data buffer 48 outputs the read data DQ to the data buffer 48 of the adjacent module 42A in synchronization with an output read clock RCLK_OUT signal generated based on the received write clock WCLK_IN signal.

Please replace the paragraph at page 14, lines 14-19 with the following amended paragraph:

A3

Accordingly, the data buffer 48 in this example includes three clock domains. The first clock domain is determined by the input write clock signal WCLK_IN received from an adjacent lower-order memory module, or memory controller.[[.]] The second clock domain is determined by the module read clock signal RCLK_MDL received from the local memory devices 44. The third clock domain is determined by the input read clock signal RCLK_IN received from an adjacent higher-order memory module.

Please replace the Abstract of the Disclosure at page 31 with the following amended paragraph:

ABSTRACT OF THE DISCLOSURE

A4

A clocking system and method in a point-to-point bus configuration overcomes the limitations of conventional approaches. In one embodiment, the present invention ensures the same phase relationship for the write clock in the write direction for all data transfers between modules, and similarly the same phase relationship for the read clock in the read direction for all data transfers between modules, regardless of module location. In another embodiment, on a given module, all transfers of data between a data buffer and a memory device in both read and write directions are clocked by a read clock signal and a write clock signal that have the same phase relationship and have the same propagation delay as the data bus between the buffer and the memory device.

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